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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,608	12/24/2003	CHIH-FENG SUNG	10217-US-PA	1607

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
TRAN, THUY V	
ART UNIT	PAPER NUMBER
2821	

NOTIFICATION DATE	DELIVERY MODE
03/06/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/707,608	SUNG, CHIH-FENG	
	Examiner	Art Unit	
	Thuy V. Tran	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment submitted on 12/05/2007* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-17 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-17 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Applicant's amendment submitted on 12/05/2007. In virtue of this amendment, claims 1-11, 18-20 have been canceled, and claims 12-17 and 21-24 are currently presented in the instant application.

Applicant's arguments on amended claims 12, 21, and their dependent claims filed on 12/05/2007 have been fully considered but are moot in view of the new grounds of rejection. The rejections of these claims are being made as follows:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 12-17 and 21-24 are rejected under 35 U.S.C. 102(a) as being anticipated by Asano et al. (Pub. No.: US 2002/0190924 A1; hereinafter "Asano").

With respect to claim 12, Asano discloses, in Fig. 1, an organic light-emitting display comprising (1) a pixel array having a plurality of data lines [Y(i), Y(i+1), Y(i+2)]], a plurality of scan lines [X(i), X(i+1), X(i+2)], and a plurality of first (e.g. row having data lines [Y(i, i+1,...)] and scanning lines [X(i), X(i+1)]) and second pixels (e.g. row having data line [Y(i, i+1)] and scanning lines [X(i+1), X(i+2)]), wherein each of the first and second pixels is electrically connected to one of the scan lines and one of the data lines correspondingly (e.g. PIXEL [i, i] with connections to the scan line X(i) and the data line [Y(i)]), (2) a first external power line (including the top horizontal line and line [14]), dividing into a plurality of first internal power

lines (lines connected the top horizontal line and line [14]), wherein each first internal power line is directly connected to at least two of the first pixels (see Fig. 1), (3) a second external power line (the horizontal line immediately below the top one and line [15]), dividing into a plurality of second internal power lines (lines connected the horizontal line immediately below the top one and line [15]), wherein each second internal power line is directly connected to at least two of the second pixels (see Fig. 1), and the first internal power lines and the second internal power lines are separated (see Fig. 1), and (4) a power source [Vo] electrically connected to the first and second external power lines (see Fig. 1), wherein the first external power line and the second external power line provide a same power signal (from power source [Vo]; see Fig. 1) to the first pixels and the second pixels.

With respect to claim 13, Asano discloses, in Fig. 1, that each of the first and second pixels comprises (i) a switching transistor [TRiia] having a first drain electrode, a first gate electrode, and a first source electrode, wherein the first drain electrode is coupled to one of the data lines [Yi, Y(i+1), Y(i+2)], and the first gate electrode is coupled to one of the scan lines [Xi, X(i+1), X(i+2)], (ii) a driving transistor [TRiib] having a second drain electrode, a second gate electrode, and a second source electrode, wherein the second gate electrode is coupled to the first source electrode, and the second source electrode is grounded (connected to the common ground line [15]; see Fig. 1), (iii) a storage capacitor [Cii], having a first terminal and a second terminal, wherein the first terminal is coupled to the first source electrode and the second gate electrode, and the second terminal is grounded (connected to the common ground line [15]; see Fig. 1) and coupled to the second source electrode, and (iv) a light-emitting device [ELii], having an anode

and a cathode, wherein the anode is coupled to one of the first and second internal power lines (see Fig. 1) and the cathode is coupled to the second drain electrode.

With respect to claim 14, Asano discloses, in Fig. 1, that the switching transistor [TRiia] comprises a thin film transistor (see paragraph [0030], lines 1-2).

With respect to claim 15, Asano discloses, in Fig. 1, that the driving transistor [TRiib] comprises a thin film transistor (see paragraph [0030], lines 1-2).

With respect to claim 16, Asano discloses, in Fig. 1, that the light-emitting device comprises an organic light-emitting diode [ELii] (see paragraph [0026], line 1).

With respect to claim 17, Asano discloses, in Fig. 2, that the light-emitting device [Elii] comprises a polymer light-emitting diode (since it contains a transparent conductive layer, at least, which is inherently made of polymer (transparent layer)).

With respect to claim 21, Asano discloses, in Fig. 1, an organic light-emitting display comprising (1) a pixel array having a plurality of data lines [Y(i), Y(i+1), Y(i+2)]], a plurality of scan lines [X(i), X(i+1), X(i+2)], and a plurality of first (e.g. row having data lines [Y(i, i+1,...)] and scanning lines [X(i), X(i+1)]) and second pixels (e.g. row having data line [Y(i, i+1)] and scanning lines [X(i+1), X(i+2)]) arranged in a matrix of columns and rows, wherein each of the first and second pixels is electrically connected to one of the scan lines and one of the data lines correspondingly (e.g. PIXEL [i, i] with connections to the scan line X(i) and the data line [Y(i)]), (2) a first external power line (including the top horizontal line and line [14]), dividing into a plurality of first internal power lines (lines connected the top horizontal line and line [14]), wherein each first internal power line is directly connected to at least two of the first pixels (see Fig. 1) in the row, (3) a second external power line (the horizontal line immediately below the

top one and line [15]), dividing into a plurality of second internal power lines (lines connected the horizontal line immediately below the top one and line [15]), wherein each second internal power line is directly connected to the second pixels (see Fig. 1) in the same row, wherein the first internal power lines and the second internal power lines are separated (see Fig. 1), and (4) a power source [Vo] electrically connected to the first and second external power lines (see Fig. 1), wherein the first external power line and the second external power line provide a same power signal (from power source [Vo]; see Fig. 1) to the first pixels and the second pixels.

With respect to claim 22, Asano discloses, in Fig. 1, that each of the first and second pixels comprises (i) a switching transistor [TRiia] having a first drain electrode, a first gate electrode, and a first source electrode, wherein the first drain electrode is coupled to one of the data lines [Yi, Y(i+1), Y(i+2)], and the first gate electrode is coupled to one of the scan lines [Xi, X(i+1), X(i+2)], (ii) a driving transistor [TRiib] having a second drain electrode, a second gate electrode, and a second source electrode, wherein the second gate electrode is coupled to the first source electrode, and the second source electrode is grounded (connected to the common ground line [15]; see Fig. 1), (iii) a storage capacitor [Cii], having a first terminal and a second terminal, wherein the first terminal is coupled to the first source electrode and the second gate electrode, and the second terminal is grounded (connected to the common ground line [15]; see Fig. 1) and coupled to the second source electrode, and (iv) a light-emitting device [ELii], having an anode and a cathode, wherein the anode is coupled to one of the first and second internal power lines (see Fig. 1) and the cathode is coupled to the second drain electrode.

With respect to claim 23, Asano discloses, in Fig. 1, that the first external power line and the second external power line are respectively disposed at two opposite sides of the whole pixel

array, wherein the first internal power lines extend into the pixel array from the first external power line, the second internal power lines extend into the pixel array from the second external power line, and the first internal power lines and the second internal power lines do not extend crossing the whole pixel array.

With respect to claim 24, Asano discloses, in Fig. 1, that the first external power line and the second external power line are respectively disposed at two opposite sides of the whole pixel array, wherein the first internal power lines extend into the pixel array from the first external power line, the second internal power lines extend into the pixel array from the second external power line, and the first internal power lines and the second internal power lines do not extend crossing the whole pixel array.

Remarks and conclusion

3. In reply to Applicant's arguments that "each of the power lines disclosed by Asano is not directly connected to at least two of the pixels" in lines 4-6 at page 8, and "each of the power lines disclosed by Asano is not directly connected to the pixels in the same column or in the same row" in lines 3-4 at page 9, it is noted that Asano apparently discloses such features. Specifically, Asano discloses, in Fig. 1, a first external power line (including the top horizontal line and line [14]), which divides into a plurality of first internal power lines (lines connected the top horizontal line and line [14]), wherein each first internal power line is directly connected to at least two of the first pixels (see Fig. 1) in the row, and a second external power line (the horizontal line immediately below the top one and line [15]), which divides into a plurality of second internal power lines (lines connected the horizontal line immediately below the top one

and line [15]), wherein each second internal power line is directly connected to the second pixels (see Fig. 1) in the same row.

4. In reply to Applicant's arguments that "Asano fails to disclose the limitation "the first external power line and the second external power line are respectively disposed at two opposite sides of the whole pixel array… and the first internal power lines and the second internal power lines do not extend crossing the whole pixel array" in lines 4-7 at page 10, it is noted that Asano apparently discloses such features. Specifically, Asano discloses, in Fig. 1, that the first external power line (including the top horizontal line and line [14]) and the second external power line (the horizontal line immediately below the top one and line [15]) are respectively disposed at two opposite sides of the whole pixel array, wherein the first internal power lines (lines connected the top horizontal line and line [14]) extend into the pixel array from the first external_power line, the second internal power lines connected the horizontal line immediately below the top one and line [15]) extend into the pixel array from the second external_power line, and the first internal power lines and the second internal power lines do not extend crossing the whole pixel array.

For the aforementioned, claims 12-17 and 21-24 are now rejected under 35 U.S.C. 102(a) as being anticipated by Asano (see "Claim Rejections – 35 USC § 102" set forth above for details).

5. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuy V. Tran whose telephone number is (571) 272-1828. The examiner can normally be reached on M-F (8:00 AM -4:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Owens W. Douglas can be reached on (571) 272-1662. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thuy Vinh Tran/
Primary Examiner, Art Unit 2821